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APPLICATION NO.	FI	LING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/114,504	4,504 07/13/1998		ELIYAHOU HARARI	9326	
36257	7590	12/03/2004		EXAMINER	
PARSONS	HSUE &	DE RUNTZ LLP	LE, VU ANH		
655 MONTO SUITE 1800		STREET	ART UNIT	PAPER NUMBER	
SAN FRANCISCO, CA 94111				2824	
				DATE MAIL ED: 12/03/200	1

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)					
	09/114,504	HARARI ET AL.					
Office Action Summary	Examiner	Art Unit					
	Vu A. Le	2824					
The MAILING DATE of this communication ap Period for Reply	pears on the cover sheet with the c	orrespondence address					
A SHORTENED STATUTORY PERIOD FOR REPL THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1. after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reple of NO period for reply is specified above, the maximum statutory period Failure to reply within the set or extended period for reply will, by statut Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	136(a). In no event, however, may a reply be timely within the statutory minimum of thirty (30) days will apply and will expire SIX (6) MONTHS from e, cause the application to become ABANDONE	nely filed s will be considered timely. the mailing date of this communication. D (35 U.S.C. § 133).					
Status							
1)⊠ Responsive to communication(s) filed on 06 N	May 2003.						
2a) This action is FINAL . 2b) ∑ This	s action is non-final.						
3) Since this application is in condition for allowa	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is						
closed in accordance with the practice under	closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.						
Disposition of Claims							
4)⊠ Claim(s) <u>63-65</u> is/are pending in the application	Claim(s) 63-65 is/are pending in the application.						
	4a) Of the above claim(s) is/are withdrawn from consideration.						
5) Claim(s) is/are allowed.							
6)⊠ Claim(s) <u>63-65</u> is/are rejected.							
7) Claim(s) is/are objected to.	Claim(s) is/are objected to.						
8) Claim(s) are subject to restriction and/o	Claim(s) are subject to restriction and/or election requirement.						
Application Papers							
9) The specification is objected to by the Examine	er.	•					
10)⊠ The drawing(s) filed on <u>13 July 1998</u> is/are: a)⊠ accepted or b)□ objected to by the Examiner.							
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).							
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).							
11)☐ The oath or declaration is objected to by the E	xaminer. Note the attached Office	Action or form PTO-152.					
Priority under 35 U.S.C. § 119							
12) Acknowledgment is made of a claim for foreign a) All b) Some * c) None of:		-(d) or (f).					
1. Certified copies of the priority document		N- 07/227 500					
2. Conjugate the partition conjugate the prior							
3. Copies of the certified copies of the prior	•	d in this National Stage					
application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received.							
and analytica detailed emot detion for a list	. S. M. SS. Miloga Sopies Hat receive	•					
Attachment(c)							
Attachment(s) 1) Notice of References Cited (PTO-892)	4) Interview Summary	(PTO-413)					
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Da	te					
 Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>09/08/03</u>. 	5) Notice of Informal Page 6) Other:	atent Application (PTO-152)					

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DETAILED ACTION

Claim Rejections - 35 USC § 112

- 1. The following is a quotation of the first paragraph of 35 U.S.C. 112:
 - The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.
- 2. Claims 63-65 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.
- 3. Claims 63-65 recite "a data control logic circuit for controlling a transfer of data ... and respectively transmitting block erase commands..." The specification fails to support the data control logic circuit. The controller (31 in Figures.1A, 1B, 2, 6 and 7) can controlling a transfer of data and transmitting block erase command but this controller is not a part of the flash memory card (33) as claimed in the claims 63-65. The controller is outside of the flash memory card and controls the flash memory card through connectors (35 and 39). The circuit (220) in Figure.3A does not control a transfer of data. That circuit transfers erase address and erase commands only. Figures 6-8 do not disclose any thing about erase circuit.
- 4. The specification also fails to disclose an address control logic circuit for managing addresses and for respectively transmitting chip enable signal to at least two

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of the plurality of flash memory partitions including the physical blocks to be erased. The address control logic circuit transmits chip enable signals to selected chips containing tagged physical blocks to be erased only, not to all flash memory chips. The erase circuit 220 (in Figure 3A) transmits a global erase command to all flash memory chips (see page 10, lines 32-35). For example the specification said that "after all sectors intended for erase have been selected, the controller then issues to the circuit 220, as well as all other chips in the system a global erase command in line 251".

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vu A. Le whose telephone number is (571) 272-1871. The examiner can normally be reached on M-F (7:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vu A. Le

Primary Examiner
Art Unit 2824

11/30/04